EXPRESS MAILING LABEL
NO. EV133103527US

PATENTS
174/198 Div.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Martin Langhammer
Application No.	:	Not Yet Assigned
Filed	:	Herewith
For	:	PROGRAMMABLE LOGIC DEVICES WITH FUNCTION-SPECIFIC BLOCKS
Group Art Unit	:	Not Yet Assigned
Examiner	:	Not Yet Assigned

Mail Stop PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicant wishes to call the attention of the Examiner to the following references:

U.S. PATENTS

3,473,160	Wahlstrom	Oct. 14, 1969
4,871,930	Wong et al.	Oct. 03, 1989
5,122,685	Chan et al.	June 16, 1992
5,128,559	Steele	July 07, 1992
5,371,422	Patel et al.	Dec. 06, 1994
5,483,178	Costello et al.	Jan. 09, 1996
5,570,039	Oswald et al.	Oct. 29, 1996
5,689,195	Cliff et al.	Nov. 18, 1997
5,754,459	Telikepalli	May 19, 1998
5,825,202	Tavana et al.	Oct. 20, 1998
5,874,834	New	Feb. 23, 1999
5,999,015	Cliff et al.	Dec. 07, 1999
6,069,487	Lane et al.	May 30, 2000

6,215,326 B1	Jefferson et al.	Apr. 10, 2001
6,407,576	Ngai et al.	Jun. 18, 2002
2002/0089348	Langhammer	Jul. 11, 2002
6,538,470	Langhammer et al.	Mar. 25, 2003
6,556,044	Langhammer et al.	Apr. 29, 2003

FOREIGN PATENTS

0 461 798 A2	EPO	Dec. 18, 1991
2 283 602 A	GB	May 10, 1995

OTHER DOCUMENTS

"Implementing Multipliers in FLEX 10K EABs", Altera, March 1996.

"Xilinx Unveils New FPGA Architecture to Enable High-Performance, 10 Million System Gate Designs", Xilinx , June 22, 2000.

"Xilinx Announces DSP Algorithms, Tools and Features for Virtex-II Architecture", Xilinx, November 21, 2000.

"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, January 25, 2001, module 2 of 4.

"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, April 2, 2001, module 1 of 4.

"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, April 2, 2001, module 2 of 4.

"Implementing Logic with the Embedded Array in FLEX 10K Devices", Altera, May 2001, ver. 2.1.

"The QuickDSP Design Guide", Quicklogic, August 2001, revision B.

"QuickDSP™ Family Data Sheet", Quicklogic, August 7, 2001, revision B.

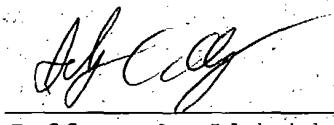
These references, which are listed on the accompanying form PTO-1449 (submitted in duplicate), were either cited by or submitted to the United States Patent Office in application No. 09/924,354, from which the present application claims

priority under 35 U.S.C. § 120. Pursuant to 37 C.F.R. § 1.98(d), no copies of the references are being provided herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

It is respectfully requested that these documents be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicant respectfully requests that a copy of Form PTO-1449, as considered and initialed by the Examiner, be returned with the next communication.

Respectfully submitted,



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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 174/198 Div.	APPLICATION NO. Not Yet Assigned
	APPLICANT Martin Langhammer	CONFIRMATION NO. Not Yet Assigned
	FILING DATE Herewith	GROUP Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,473,160	10/14/69	Wahlstrom	340	172.5	
	4,871,930	10/03/89	Wong et al.	307	465	
	5,122,685	06/16/92	Chan et al.	307	465.1	
	5,128,559	07/07/92	Steele	307	465	
	5,371,422	12/06/94	Patel et al.	326	41	
	5,483,178	01/09/96	Costello et al.	326	41	
	5,570,039	10/19/96	Oswald et al.	326	39	
	5,689,195	11/18/97	Cliff et al.	326	41	
	5,754,459	05/19/98	Telikepalli	364	759	
	5,825,202	10/20/98	Tavana et al.	326	39	
	5,874,834	02/23/99	New	326	39	
	5,999,015	12/07/99	Cliff et al.	326	39	
	6,069,487	05/30/00	Lane et al.	326	37	
	6,215,326 B1	04/10/01	Jefferson et al.	326	41	
	6,407,576	06/18/02	Ngai et al.	326	41	
	2002/0089348	07/11/02	Langhammer	326	38	
	6,538,470	03/25/03	Langhammer et al.	326	41	
	6,556,044	04/29/03	Langhammer et al.	326	40	

FOREIGN PATENT APPLICATIONS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	0 461 798 A2	12/18/91	EPO	H03K	19/177		
	2 283 602 A	05/10/95	GB	H03K	19/177		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	"Implementing Multipliers in FLEX 10K EABs", Altera, March 1996.
	"Xilinx Unveils New FPGA Architecture to Enable High-Performance, 10 Million System Gate Designs", Xilinx, June 22, 2000.
	"Xilinx Announces DSP Algorithms, Tools and Features for Virtex-II Architecture", Xilinx, November 21, 2000.
	"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, January 25, 2001, module 2 of 4.
	"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, April 2, 2001, module 1 of 4.
	"Virtex-II 1.5V Field-Programmable Gate Arrays", Xilinx, April 2, 2001, module 2 of 4.
	"Implementing Logic with the Embedded Array in FLEX 10K Devices", Altera, May 2001, ver. 2.1.
	"The QuickDSP Design Guide", Quicklogic, August 2001, revision B.
	"QuickDSP™ Family Data Sheet", Quicklogic, August 7, 2001, revision B.

EXAMINER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

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